ABSTRACT OF THE DISCLOSURE

This inventing is intended to shorten data deletion time of a nonvolatile semiconductor memory such as a flash memory (EEPROM). When deleting data written to a memory cell MC0 among flash memory cells MC0 to MC2 formed on a semiconductor substrate PSUB through a separation region NiSO, a voltage of p type well PWL0 in which the memory cell MC0 is formed is raised to 10V and a voltage of the separation region NiSO is raised to 12V by using a voltage application unit different from a voltage application unit applying a voltage to the p type well PWL0. As a result, parasitic capacitances Ca_1 and Ca_2 generated between p type wells PWL1 and PWL2 in which the unselected memory cells MC1 and MC2 are formed and the separation region NiSO, respectively, and a parasitic capacitance Cb generated between the separation region NiSO and the semiconductor substrate PSUB are charged by the voltage application units. It is, therefore, possible to shorten time required to charge the parasitic capacitances and to shorten the deletion time.